REMARKS/ARGUMENTS

Notation to the amendments

The Examiner has noted that text deleted must be shown by strikethrough unless the strikethrough is not clear, such as in the case of a comma. In such case, the deleted text should be surrounded by double brackets. Applicant has amended the claims where the strikethrough is not clear to indicate deleted text by using double brackets, as suggested by the Examiner.

The Examiner has also noted that the status "currently amended" may not accurately reflect the status of the claims. Applicant has amended the status, where appropriate to reflect the correct status of the claims.

Allowable Subject Matter

Claims 2-3, 8-10, 16-18, 19, 22, and 32-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. To expedite prosecution, Applicant has amended claim 2 to be in independent form and to include all limitations of the base claim and any intervening claims. As for claim 12, it has been amended to include all limitations of claim 16 as well as to more clearly recite the invention. Therefore, Applicant submits that claims 2 and 12 are now allowable. Since claims 3-10 and 14-21 are or have been amended to be directly or indirectly dependent on either claim 2 or 12, these claims are also allowable. Claims 11 and 21, by way of this response, have been cancelled without prejudice.

Rejections under 35 USC § 102

Claims 1, 4-7, 11-12, 14-15, 20-21 and 23-31 are rejected under 35 USC § 102(b) as being anticipated by Uchida et al. (U.S. Patent No. 6,359,813). Applicants submit that the rejection to claims 4-7, 11-12, 14-15 and 20-21 are moot in view of the amendments to claims 2 and 12. As for claims 1 and 23-31, Applicant respectfully disagrees.

Claim 1, as amended to more clearly define the invention, recites a memory device having a plurality of memory cells, each memory cell includes first and second ports forming a memory array with first and second access ports. The first access port is an external port for read and write memory accesses and the second access port is an internal port for refresh operations. A refresh control unit is provided for generating refresh control signals to control refreshing of the memory cells. A contention detection circuit is provided to, when a memory access via the external port and a refresh operation via the internal port occur, compares an access row address of the memory access with a refresh row address of the refresh operation and suppressing the refresh operation if the access row address and the refresh address are equal.

Uchida describes a memory device. However, unlike the memory device of claim 1, Uchida's memory cells are single port memory cells, forming a single access port memory array. Uchida nowhere teaches or suggests memory cells having first and second ports forming a memory array with first and second access ports. Although Uchida describes a refresh address counter which provides a refresh address, both memory access address and refresh address are provided to the memory array through the same port. Specifically, either the refresh row address or the memory access row address is provided to the row decoder through a select circuit. See Uchida et al., Figures 5A-5B, element 45.

Furthermore, the Examiner suggests that the control circuit of Uchida (Fig. 1B, element 121 and col. 4, lines 40-62) is the same as the contention circuit of claim 1. See Office Action mailed August 31, 2004, page 3. Applicant again respectfully disagrees. The control circuit, as described by Uchida, generates a refresh control signal which is supplied to the refresh address counter and address selector switch. In normal operation (read/write operation), the address selector switch passes the external address of the memory access to the array; in refresh mode, the address selector switch passes an internal address generated by the refresh address counter to the array. See Uchida, col. 4, lines 53-60 and Fig. 1B.

However, Uchida nowhere teaches or suggests that the control circuit compares a row address of the memory access with a refresh address to determine if they are equal or not as recited by claim 1. This is because the control circuit receives neither the row address of the memory access nor the refresh address. In addition, as with conventional memory ICs, when the control circuit generates an active refresh control signal, it goes into refresh mode. In refresh mode, memory accesses are blocked until refresh is completed. This is in contrast with the memory device claim 1 which suppresses or blocks the refresh operation when the access row address and the refresh address are equal (e.g., contention between refresh and memory access). Therefore, Applicant submits that claim 1 is patentable over Uchida.

With respect to claim 23, it recites an IC comprising a multi-port memory cell array having at least first and second ports and a contention detection circuit for detecting contention between a refresh operation from one of the ports and a read or write memory access operation from the other of the ports and suppressing the refresh operation when contention occurs to allow the read or write memory access to execute. Applicant submits that Uchida neither teaches nor

suggests a multi-port memory cell array or a contention circuit which suppresses the refresh operation when contention occurs between a memory access in one of the first and second ports and a refresh operation in other of the first and second ports to allow the read or write memory access to execute. See above discussion regarding claim 1. Therefore, Applicant submits that claim 23 is patentable over Uchida. Since claims 24-35 and newly added claims 36-39 are directly or indirectly dependent on claim 23, these claims are also patentable.

With respect to newly added claim 40, it recites an IC having a plurality of memory cells forming an array arranged in rows and columns. The IC includes a contention detection circuit, which when a read or write memory access and a refresh operation are to the same row of memory cells, suppresses the refresh operation to enable execution of the read or write memory access. Applicant submits that Uchida nowhere teaches or suggests a contention detection circuit which suppresses the refresh operation to enable execution of the read or write memory access when a read or write memory access and a refresh operation occur to the same row of memory cells. See above discussion regarding claim 1. Therefore, Applicant submits that claim 40 is patentable over Uchida. Since claim 41 is dependent on claim 40, this claim is also patentable.

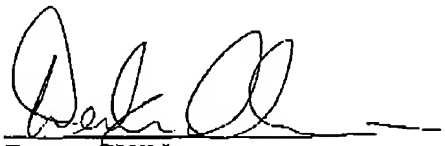
Conclusion

In view of the foregoing, Applicant believes that all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: January 31, 2004

Respectfully submitted,



Dexter CHIN
Attorney for Applicant
Reg. No. 38,842

Horizon IP Pte Ltd
8 Kallang Sector,
East Wing 7th Floor
Singapore 349282
Tel.: (65) 9836 9908
Fax: (65) 6846 2005